

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Magdy Abadir et al.	) Examiner: Unknown	PRE A
Application No.: 09/781,492	) Art Unit: Unknown	10 CE 14
•	) Docket No.: SC11403TS	CENTER 2800
Filed: February 13, 2001	) Date: March 26, 2001 )	ER 26
Title: DESIGN ANALYSIS TOOL FOR PATH	)	00
EXTRACTION AND FALSE PATH	)	•
IDENTIFICATION AND METHOD		
THEREOF		
Assistant Commissioner for Patents		
Washington, DC 20231		

## SUBMISSION OF INFORMATION DISCLOSURE STATEMENT

## Dear Assistant Commissioner:

larch 26, 2001

In compliance with 37 C.F.R. 1.98, Applicants are herein submitting a copy of related subject matter found in a public reference. In particular, pages 163-166 are being submitted from a book authored by Alfred L. Crouch entitled <u>Design-for-Test for Digital IC's and Embedded Core Systems</u> (1999 Prentice Hall PTR). No fee should be associated with this communication.

Respectfully submitted,

Date

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelop addressed to: Assistant Commissioner for Patents, Washington D.C. 20231 on:

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Printed or Typed Name